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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,509	10/07/2003	James M. Cleeves	MA-108	9643

7590 10/06/2005

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EXAMINER	
PERALTA, GINETTE	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,509	CLEEVES ET AL.	
	Examiner	Art Unit	
	Ginette Peralta	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62* is/are pending in the application.

4a) Of the above claim(s) *1-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/7/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 7/18/05.

2. Applicant's election with traverse of claims 7-62 in the reply filed on 7/18/05 is acknowledged. The traversal is on the ground(s) that the crystallized region having adjacent nucleation sites could only be obtained by the method of Group II. This is not found persuasive because by using a mask the nucleation sites adjacent to each other could still be formed by a plasma or by introducing other crystallizing agents to the whole surface and then using a mask to determine the nucleation sites.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 26 and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 26 depends on claim 24,which recites that the crystallizing agent is silicon nuclei, while claim 26 recites that the crystallizing agent is germanium, it is indefinite

whether the crystallizing agent is silicon nuclei or germanium and this renders the claims 26 and 27 indefinite.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 7, 11-13, 17, 22-23, 26-27, 30, 32, 34-35, 43-46, and 62 are rejected under 35 U.S.C. 102(b) as being anticipated by Park et al. (U. S. Pat. 6,727,514 B2).

Regarding claim 7, Park et al. discloses a method for crystallizing a polysilicon layer on a wafer that comprises forming a first amorphous silicon layer, as disclosed in col. 6, lines 49-54; selectively introducing a crystallizing agent on the amorphous layer in a substantially symmetric pattern in two dimensions, as shown in Fig. 1(a); and annealing the wafer to form the crystallized polysilicon layer, wherein substantially no amorphous silicon remains between silicon grains in the polysilicon layer, as disclosed in col. 7, lines 58-65.

Regarding claim 11, Park et al. discloses in col. 6, lines 32-40 that the crystallizing agent is germanium.

Regarding claim 12, Park et al. discloses that the step of selectively introducing a crystallizing agent comprises forming a mask layer on the first amorphous silicon layer;

etching holes in the mask layer, the holes distributed in a substantially symmetric pattern in two dimensions and exposing portions of the first amorphous layer; and depositing germanium on the mask layer and the exposed portions of the first amorphous layer, as disclosed in col. 6, lines 54-60.

Regarding claim 13, Park et al. discloses that before the annealing step, a second layer of amorphous silicon is formed on and in contact with the first amorphous silicon layer and the germanium, as disclosed in col. 7, lines 10-16.

Regarding claim 17, Park et al. discloses that a plurality of thin film transistors is formed having channel regions formed in the polysilicon layer, as disclosed in col. 8, lines 24.

Regarding claim 22, Park et al. discloses a method for producing a crystallized silicon layer with controlled defect density that comprises forming a first amorphous silicon layer on the wafer, as disclosed in col. 6, lines 49-54; selectively introducing a crystallizing agent on the amorphous layer in a substantially symmetric pattern across a seeded area, as shown in Fig. 1(a); and annealing the amorphous silicon layer, wherein after the annealing step, in the seeded area, an area bounded by adjacent nucleation sites encloses no more than five crystal grain boundaries, as shown in Figs. 1(c) and 1(d).

Regarding claim 23, Park et al. discloses that the symmetric pattern is substantially evenly spaced in two dimensions, as shown in Figs. 1(a), 2(a) and 2(b).

Regarding claim 26, Park et al. discloses in col. 6, lines 32-40 that the crystallizing agent is germanium.

Regarding claim 27, Park et al. discloses that before the annealing step, a second layer of amorphous silicon is formed on and in contact with the first amorphous silicon layer and the germanium, as disclosed in col. 7, lines 10-16.

Regarding claim 30, Park et al. discloses a method for controlling grain uniformity on a wafer that comprises forming a first layer of amorphous silicon on the wafer, as disclosed in col. 6, lines 49-54; selectively introducing a crystallizing agent at a substantially uniform intervals across an area of the amorphous silicon layer, as disclosed in Figs. 1(a), 2(a), and 2(b), and in col. 6, lines 61-67; forming a second layer of amorphous silicon on and in contact with at least portions of the first layer of amorphous silicon, as disclosed in col. 7, lines 10-16; and annealing the wafer to convert the amorphous silicon layers to a polysilicon layer, as disclosed in col. 7, lines 18-30.

Regarding claim 32, Park et al. discloses in col. 6, lines 32-40 that the crystallizing agent is germanium.

Regarding claim 34, Park et al. discloses in Figs. 1(a), 2(a), and 2(b) that the uniform intervals are substantially evenly spaced in two dimensions.

Regarding claim 35, Park et al. discloses that a plurality of thin film transistors is formed having channel regions formed in the polysilicon layer, as disclosed in col. 8, lines 24.

Regarding claim 43, Park et al. discloses a method for maximizing grain size and controlling density of grain boundaries in silicon; the method comprising forming a first amorphous silicon layer, as disclosed in col. 6, lines 49-54; selectively creating nucleation sites at uniform intervals on the amorphous silicon layer; annealing the wafer to form polysilicon wherein substantially no amorphous silicon remains between silicon grains, as disclosed in col. 7, lines 57-65; and forming a plurality of active devices, the devices at least partially formed in the polysilicon.

Regarding claim 44, Park et al. discloses a method for controlling grain boundaries in a polysilicon layer; the method comprising forming a first amorphous silicon layer on a wafer, as disclosed in col. 6, lines 49-54; forming a mask layer having holes at substantially uniform intervals on and in contact with the first amorphous silicon layer wherein the amorphous silicon layer is exposed in the holes, as disclosed in col. 6,lines 54-67; depositing a crystallizing agent on the mask layer and on the first amorphous silicon layer; forming a second amorphous silicon layer in contact with at least a portion of the first amorphous silicon layer; and annealing the wafer, as disclosed in col. 7, lines 10-30.

Regarding claim 45, Park et al. discloses that the holes are substantially evenly distributed in two dimensions, as shown in Figs. 1(a), 2(a), and 2(b).

Regarding claim 46, Park et al. discloses in col. 6, lines 32-40 that the crystallizing agent is germanium.

Regarding claim 62, Park et al. discloses a method for controlling grain boundaries in a polysilicon layer that comprises forming a first amorphous silicon layer on a wafer; forming a mask layer on and in contact with the first amorphous silicon layer; etching the mask layer wherein portions of the amorphous silicon layer are exposed; depositing silicon nuclei on the mask layer and on the first amorphous silicon layer; forming a second amorphous silicon layer in contact with at least portions of the first amorphous silicon layer; and annealing the wafer, as disclosed in col. 6, line 49 to col. 7, line 30.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 8-10, 18-21, 24, 25, 31, 36-40, 42, 47-49, 53-59, and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. in view of Yonehara (U. S. Pat. 5,457,058).

Regarding claims 8, 24, 31, and 47, Park et al. as applied above discloses the claimed invention with the exception of the crystallizing agent being silicon nuclei.

Yonehara discloses a method for crystallizing a polysilicon layer on a wafer that comprises forming a first amorphous silicon layer; selectively introducing a

crystallizing agent on the amorphous layer and annealing the wafer to form the crystallized polysilicon layer, wherein the crystallizing agent is silicon nuclei, and it is taught for the disclosed intended purpose of forming a residual crystal fine region free from injection damage at a desired position within the amorphous film, and through annealing enlarging the fine region which results in a larger grained polysilicon which is desirable for the manufacture of the devices.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use silicon nuclei as taught by Yonehara in the invention of Park et al. for the disclosed intended purpose of forming a residual crystal fine region free from injection damage at a desired position within the amorphous film, and through annealing enlarging the fine region which results in a larger grained polysilicon which is desirable for the manufacture of the devices.

Regarding claim 9, Park et al. discloses that the step of selectively introducing a crystallizing agent comprises forming a mask layer on the first amorphous silicon layer; etching holes in the mask layer, the holes distributed in a substantially symmetric pattern in two dimensions and exposing portions of the first amorphous layer; and depositing germanium on the mask layer and the exposed portions of the first amorphous layer, as disclosed in col. 6, lines 54-60.

Regarding claims 10, 25, Park et al. discloses that before the annealing step, a second layer of amorphous silicon is formed on and in contact with the first amorphous silicon layer and the crystallizing agent, as disclosed in col. 7, lines 10-16.

Regarding claims 18, 19, 20, 21, 36 and the limitations of the type of device, it has been held that to be entitled to weight in method claims, the recited-structure limitations therein must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure. Ex parte Pfeiffer, 1962 C.D. 408 (1961).

Regarding claims 37, 42 and 53, Park et al. discloses a method for maximizing grain size and controlling density of grain boundaries in silicon; the method comprising forming a first amorphous silicon layer, as disclosed in col. 6, lines 49-54; selectively creating nucleation sites at uniform intervals on the amorphous silicon layer; annealing the wafer to form polysilicon wherein substantially no amorphous silicon remains between silicon grains, as disclosed in col. 7, lines 57-65; and forming a plurality of active devices, the devices at least partially formed in the polysilicon.

Park et al. discloses the claimed invention with the exception of forming a plurality of memory cells in the polysilicon, although active devices are formed in the polysilicon, it has been held that to be entitled to weight in method claims, the recited-structure limitations therein must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure. Ex parte Pfeiffer, 1962 C.D. 408 (1961).

Regarding claim 38, Park et al. discloses in Figs. 1(a), 2(a), and 2(b) that the uniform intervals are substantially evenly spaced in two dimensions.

Regarding claims 39, Park et al. as applied above discloses the claimed invention with the exception of the crystallizing agent being silicon nuclei.

Yonehara discloses a method for crystallizing a polysilicon layer on a wafer that comprises forming a first amorphous silicon layer; selectively introducing a crystallizing agent on the amorphous layer and annealing the wafer to form the crystallized polysilicon layer, wherein the crystallizing agent is silicon nuclei, and it is taught for the disclosed intended purpose of forming a residual crystal fine region free from injection damage at a desired position within the amorphous film, and through annealing enlarging the fine region which results in a larger grained polysilicon which is desirable for the manufacture of the devices.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use silicon nuclei as taught by Yonehara in the invention of Park et al. for the disclosed intended purpose of forming a residual crystal fine region free from injection damage at a desired position within the amorphous film, and through annealing enlarging the fine region which results in a larger grained polysilicon which is desirable for the manufacture of the devices.

Regarding claim 40, Park et al. discloses in col. 6, lines 32-40 that the step for creating nucleation sites comprises depositing germanium.

Regarding claim 48, Park et al. discloses in col. 7, lines 10-30 that the conversion of the first amorphous layer to hemispherical grains before formation of the second

layer is substantially prevented, and wherein the first and second amorphous layers are crystallized to form the polysilicon layer after the annealing step.

Regarding claim 49, Park et al. discloses the claimed invention with the exception of forming a plurality of memory cells in the polysilicon, although active devices are formed in the polysilicon, it has been held that to be entitled to weight in method claims, the recited-structure limitations therein must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure. Ex parte Pfeiffer, 1962 C.D. 408 (1961).

Regarding claim 54, Park et al. discloses a method for producing a wafer having a crystallized silicon layer with controlled defect density that comprises forming a first amorphous silicon layer on a wafer; selectively introducing a crystallizing agent on the amorphous silicon layer in a substantially symmetric pattern across a seeded area, the seeded area having a first distance between nucleation sites; and annealing the wafer, wherein after the annealing step, in the seeded area, a chance that a square area having a side less than about one fourth of the first distance has no more than one grain boundary is undetermined.

Park et al. discloses the claimed invention with the exception of disclosing the chance that a square area having a side less than about one fourth of the first distance has no more than one grain boundary being greater than about 0.75. It would have been obvious to one of ordinary skill in the art at the time the invention was made to vary temperature of the annealing, the availability of the crystallizing agent and the time of

annealing, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a seeded area having the chance that a square area having a side less than about one fourth of the first distance has no more than one grain boundary being greater than about 0.75 as there is no statement denoting the criticality of the probability of the square area of the seeded area.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

Regarding claim 55, Park et al. discloses in Figs. 1(a), 2(a), and 2(b) that the uniform intervals are substantially evenly spaced in two dimensions.

Regarding claim 56, Park et al. as applied above discloses the claimed invention with the exception of the crystallizing agent being silicon nuclei.

Yonehara discloses a method for crystallizing a polysilicon layer on a wafer that comprises forming a first amorphous silicon layer; selectively introducing a crystallizing agent on the amorphous layer and annealing the wafer to form the crystallized polysilicon layer, wherein the crystallizing agent is silicon nuclei, and it is taught for the disclosed intended purpose of forming a residual crystal fine region free

from injection damage at a desired position within the amorphous film, and through annealing enlarging the fine region which results in a larger grained polysilicon which is desirable for the manufacture of the devices.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use silicon nuclei as taught by Yonehara in the invention of Park et al. for the disclosed intended purpose of forming a residual crystal fine region free from injection damage at a desired position within the amorphous film, and through annealing enlarging the fine region which results in a larger grained polysilicon which is desirable for the manufacture of the devices.

Regarding claim 57, Park et al. discloses that before the annealing step, a second layer of amorphous silicon is formed on and in contact with the first amorphous silicon layer and the crystallizing agent, as disclosed in col. 7, lines 10-16.

Regarding claim 58, Park et al. discloses in col. 6, lines 32-40 that the crystallizing agent is germanium.

Regarding claim 59, Park et al. discloses that before the annealing step, a second layer of amorphous silicon is formed on and in contact with the first amorphous silicon layer and the crystallizing agent, as disclosed in col. 7, lines 10-16.

Regarding claim 61 and the limitation of the type of device, it has been held that to be entitled to weight in method claims, the recited-structure limitations therein must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure. Ex parte Pfeiffer, 1962 C.D. 408 (1961).

9. Claims 14-16, 28-29, 33, and 50-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. in view of Lin (US Pat. Pub. 2004/0235276 A1).

Regarding claim 14, 28, and 33, Park et al. as applied above discloses the claimed invention with the exception of the crystallizing agent being laser energy.

Lin discloses a method for crystallizing a polysilicon layer on a wafer that comprises forming a first amorphous silicon layer; selectively introducing a crystallizing agent on the amorphous layer and annealing the wafer to form the crystallized polysilicon layer, wherein the crystallizing agent is laser energy, and it is taught for the disclosed intended purpose of increasing the grain size of the polysilicon film and improve the performance of the devices which is desirable for the manufacture of the devices.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use laser energy as taught by Lin in the invention of Park et al. for the disclosed intended purpose of increasing the grain size of the polysilicon film and improve the performance of the devices which is desirable for the manufacture of the devices.

Regarding claim 15, both Park et al. and Lin disclose the use of a mask to expose the amorphous silicon layer, furthermore, Park et al. discloses treating the first amorphous layer at locations distributed in a substantially symmetric pattern.

Regarding claims 16 and 29, both Park et al. and Lin disclose the use of a mask to expose the amorphous silicon layer, furthermore, Park et al. discloses treating the first

amorphous layer at locations distributed in a substantially symmetric pattern wherein a plurality of transistors are formed, and channel regions of the thin film transistors are formed in the polysilicon layer; and Lin discloses the use of a laser interference pattern.

Regarding claim 50, Park et al. discloses a method for controlling grain density in crystallized silicon that comprises forming a layer of amorphous silicon on the wafer, as disclosed in col. 6, lines 49-54; exposing the amorphous silicon layer to create symmetrically distributed nucleation sites, as disclosed in Figs. 1(a), 2(a), and 2(b), and in col. 6, lines 61-67; and annealing the wafer to convert the amorphous silicon layers to a polysilicon layer, as disclosed in col. 7, lines 18-30.

Park et al. discloses the claimed invention with the exception of exposing the amorphous silicon to laser energy.

Lin discloses a method for crystallizing a polysilicon layer on a wafer that comprises forming a first amorphous silicon layer; selectively introducing a crystallizing agent on the amorphous layer and annealing the wafer to form the crystallized polysilicon layer, wherein the crystallizing agent is laser energy, and it is taught for the disclosed intended purpose of increasing the grain size of the polysilicon film and improve the performance of the devices which is desirable for the manufacture of the devices.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use laser energy as taught by Lin in the invention of Park et al. for the disclosed intended purpose of increasing the grain size of the polysilicon film

and improve the performance of the devices which is desirable for the manufacture of the devices.

Regarding claims 51-52, Park et al. discloses the claimed invention with the exception of forming a plurality of memory cells in the polysilicon, although active devices are formed in the polysilicon, it has been held that to be entitled to weight in method claims, the recited-structure limitations therein must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure. Ex parte Pfeiffer, 1962 C.D. 408 (1961).

10. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. in view of Yonehara as applied to claims 8-10, 18-21, 24, 25, 31, 36-40, 42, 47-49, 54-59, and 61 above, and further in view of Lin.

Park et al. as modified above discloses the claimed invention with the exception of the crystallizing agent being laser energy at uniform intervals.

Lin discloses a method for crystallizing a polysilicon layer on a wafer that comprises forming a first amorphous silicon layer; selectively introducing a crystallizing agent on the amorphous layer and annealing the wafer to form the crystallized polysilicon layer, wherein the crystallizing agent is laser energy, and it is taught for the disclosed intended purpose of increasing the grain size of the polysilicon film and improve the performance of the devices which is desirable for the manufacture of the devices.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use laser energy as taught by Lin in the invention of Park et al. for the disclosed intended purpose of increasing the grain size of the polysilicon film and improve the performance of the devices which is desirable for the manufacture of the devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571) 272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GP

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